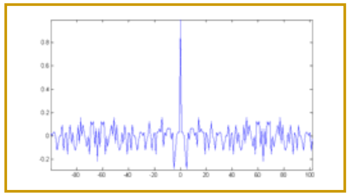
ECE 5660 – Spread Spectrum Communications
Spring 2008



Instructor: R. Michael Buehrer

Lecture #9: Code Tracking

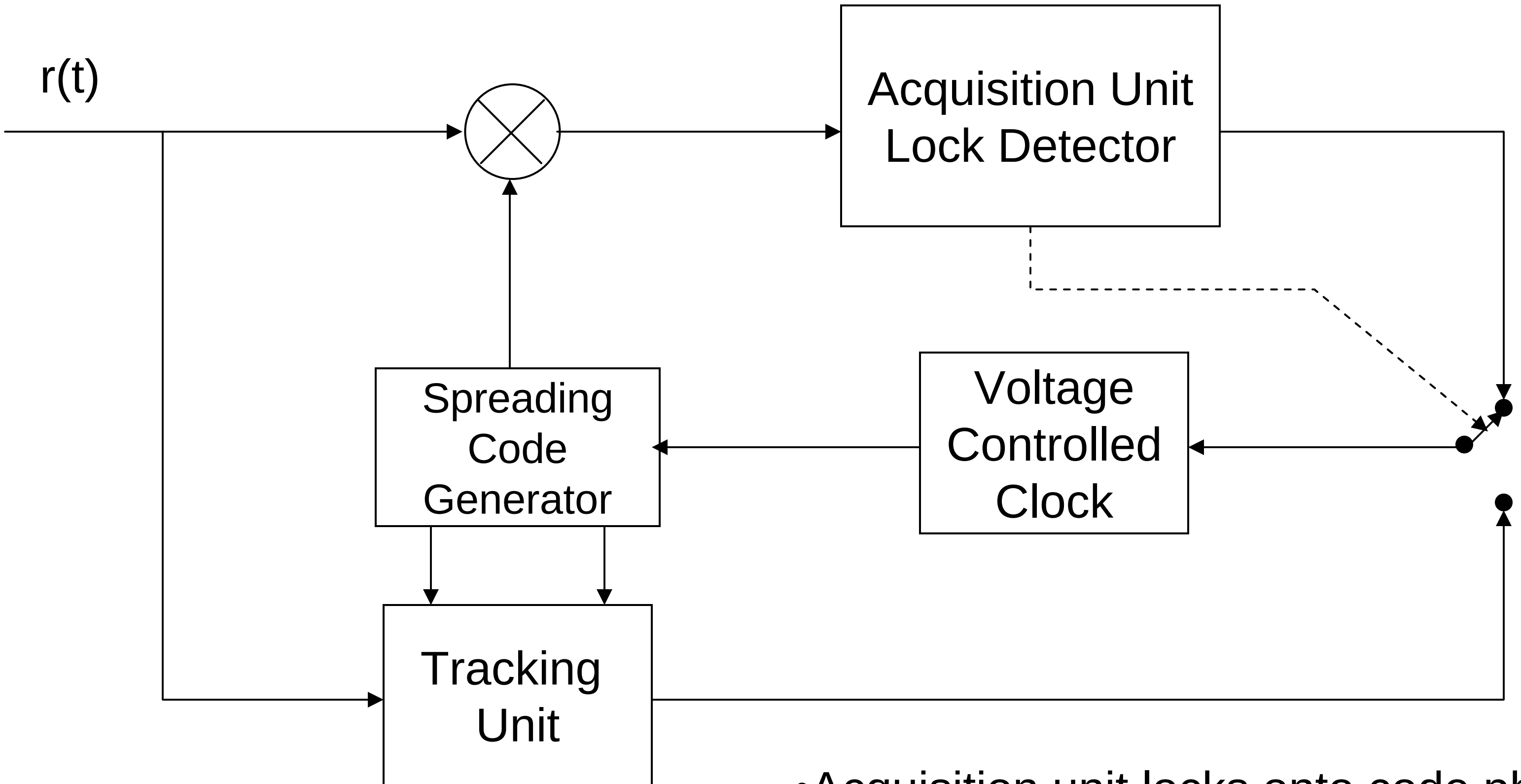
Synchronization

- All digital communications systems must perform synchronization.
- Synchronization is the process of aligning the receiver's symbol clock with the incoming waveform to optimize performance (specifically SNR).
- Traditional digital communication systems suffer from a loss of receive energy if the matched filter/correlator is sampled at the wrong time (i.e., the local version of the pulse shape is not aligned with the incoming pulse).
- Spread spectrum systems suffer from the same problem but require much more accurate sampling as a fraction of the symbol duration since an offset of T/N can reduce SNR by a factor of N^2.
- Spreading codes with good autocorrelation properties facilitate synchronization.

Synchronization

- There are two parts to the synchronization process
  - Acquisition
    - This process searches over a large space attempting to determine the timing of incoming signal.
    - Often only obtains coarse synchronization (within ½ T_c)
  - Tracking
    - This process maintains proper timing as the signal timing changes.
    - Accomplishes much finer timing adjustments
    - Fails if the offset is too large (> T_c) or changes too quickly
      - If offset changes too quickly, tracking fails and acquisition must be performed again.

Code Synchronization



- Acquisition unit locks onto code phase to within a fraction of a chip
- After lock is achieved, control of the code generator is passed to the tracker.

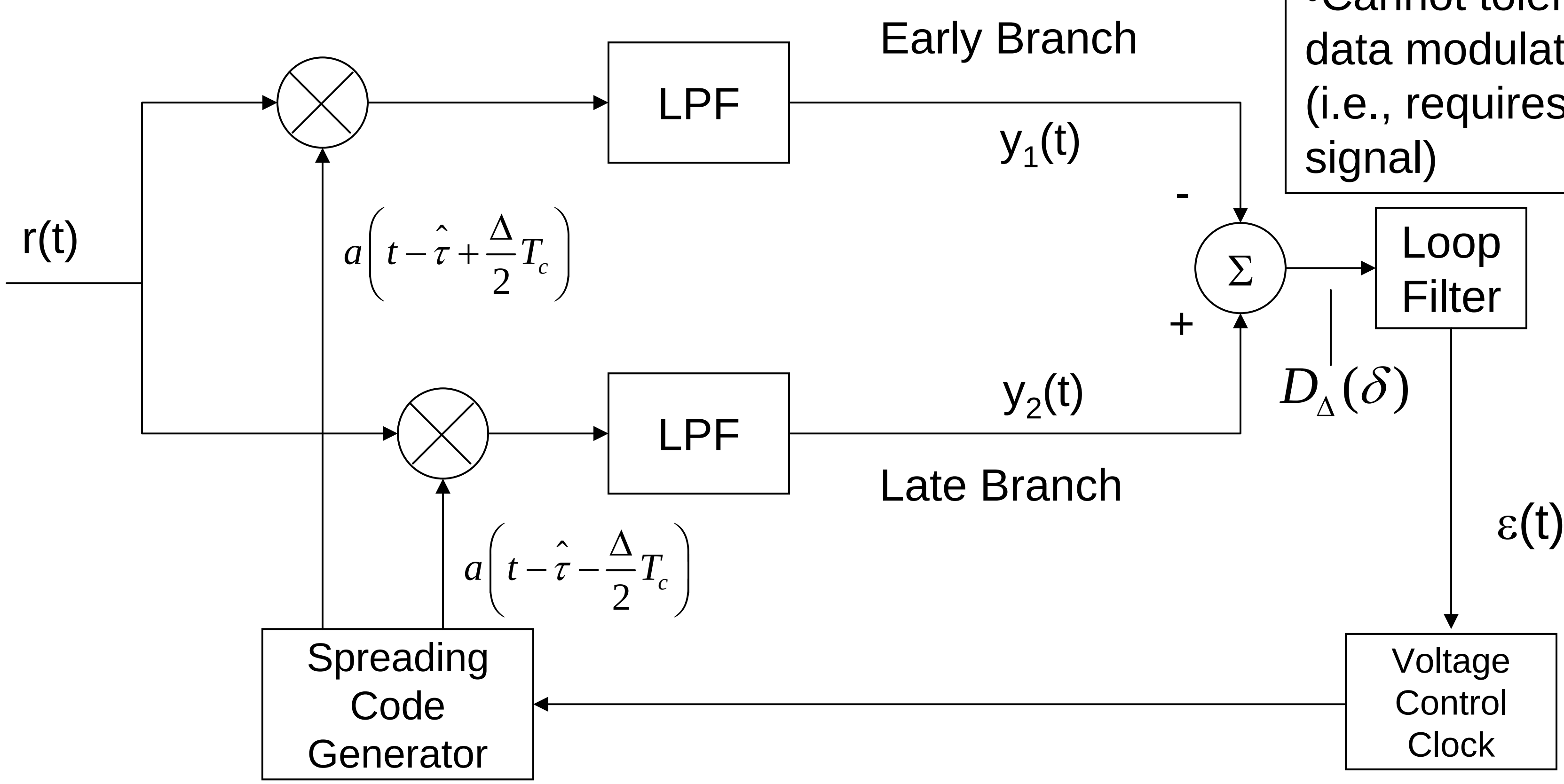
Tracking

- Code Tracking is analogous to phase tracking which is done in coherent communication systems.
- Tracking requires acquisition to obtain the timing to within a fraction of a chip period.
- The code tracking circuitry can then maintain fine synchronization.
- Several techniques for tracking
  - Delay Lock Loop
  - Tau-Dither Loop
  - Double-Dither Loop
- We will focus on the Delay Lock Loop (DLL) also known as the Early-Late Gate

Coherent Delay Lock Loop

- Coherent Early-Late Gate

•Requires phase coherence prior to tracking
•Cannot tolerate data modulation (i.e., requires a pilot signal)



Δ = branch offset in chips

Coherent Delay Lock Loop

- If we assume that the LPF filters are sliding integration windows of duration $T=NT_c$, the output of the early and late branch LPF's are

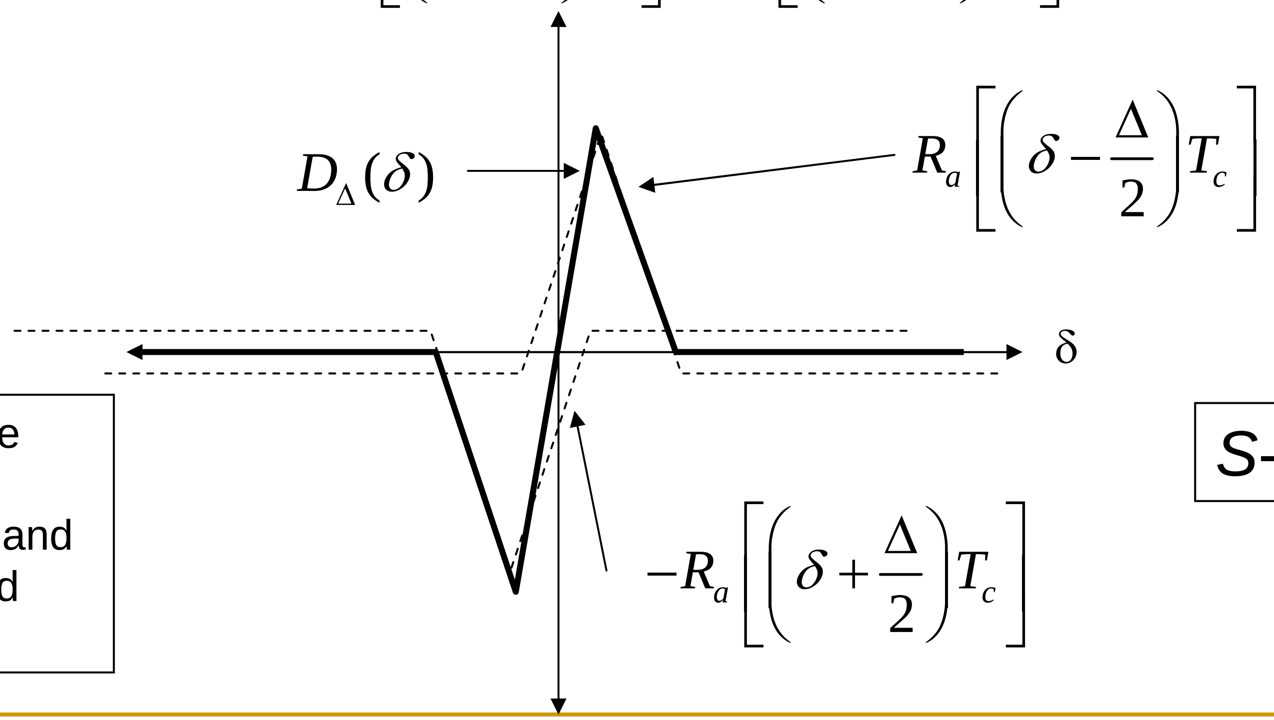
$$
\begin{aligned}
y_1(t) &= \int_t^{t+T} a\left(\lambda - \hat{\tau} + \frac{\Delta}{2}T_c\right) a(\lambda - \tau)\, d\lambda \\
&= R_a\left(\tau - \hat{\tau} + \frac{\Delta}{2}T_c\right) \\
&= R_a\left(\left[\delta + \frac{\Delta}{2}\right]T_c\right)
\end{aligned}
$$

$$
\begin{aligned}
y_2(t) &= \int_t^{t+T} a\left(\lambda - \hat{\tau} - \frac{\Delta}{2}T_c\right) a(\lambda - \tau)\, d\lambda \\
&= R_a\left(\tau - \hat{\tau} - \frac{\Delta}{2}T_c\right) \\
&= R_a\left(\left[\delta - \frac{\Delta}{2}\right]T_c\right)
\end{aligned}
$$

Delay Lock Loop Discriminator

- If we assume that the LPF filters are sliding integration windows of duration NT_c, the input to the loop filter is*

$$D_\Delta(\delta) = R_a\left[\left(\delta - \frac{\Delta}{2}\right)T_c\right] - R_a\left[\left(\delta + \frac{\Delta}{2}\right)T_c\right]$$



δ = difference between the actual delay and the estimated delay

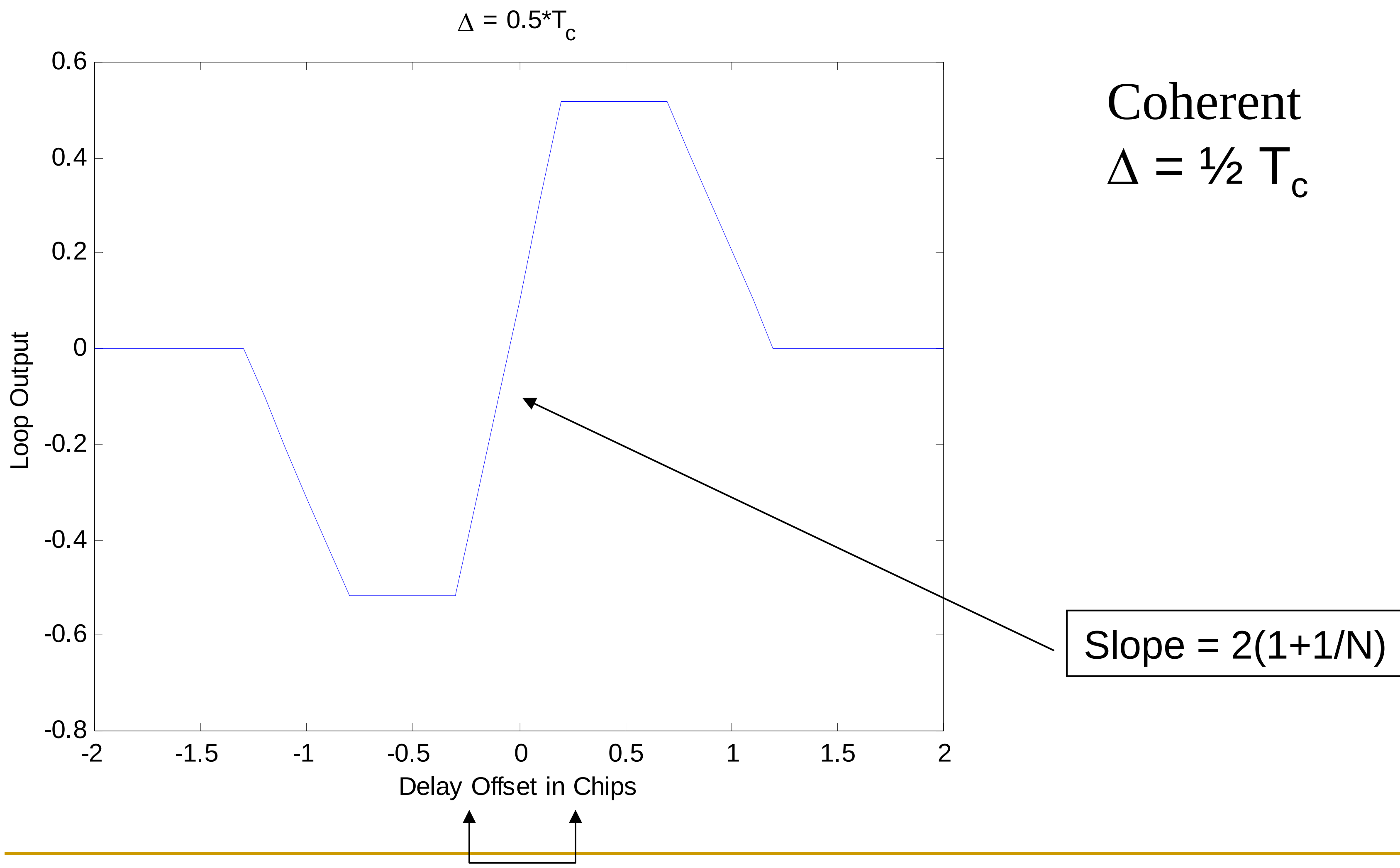
S-curve

*- Without the LPF's this is simply the DC component of the error signal.

Function of the *S*-curve

- If the output of the discriminator is > 0, the estimated delay will be increased. Is this right?
- Discriminator output > 0 means:
  - More energy in the late correlation than the early correlation
  - The estimated τ must be delayed relative to (smaller than) the actual τ
  - Thus, the actual delay should be increased
- If the output of the discriminator is < 0, the estimated delay will be decreased. Is this right?
- Discriminator output < 0 means:
  - More energy in the early correlation than the late correlation
  - The estimated τ must be advanced relative to (greater than) the actual τ
  - Thus, the actual delay should be decreased

Delay Lock Loop: *S* - curve

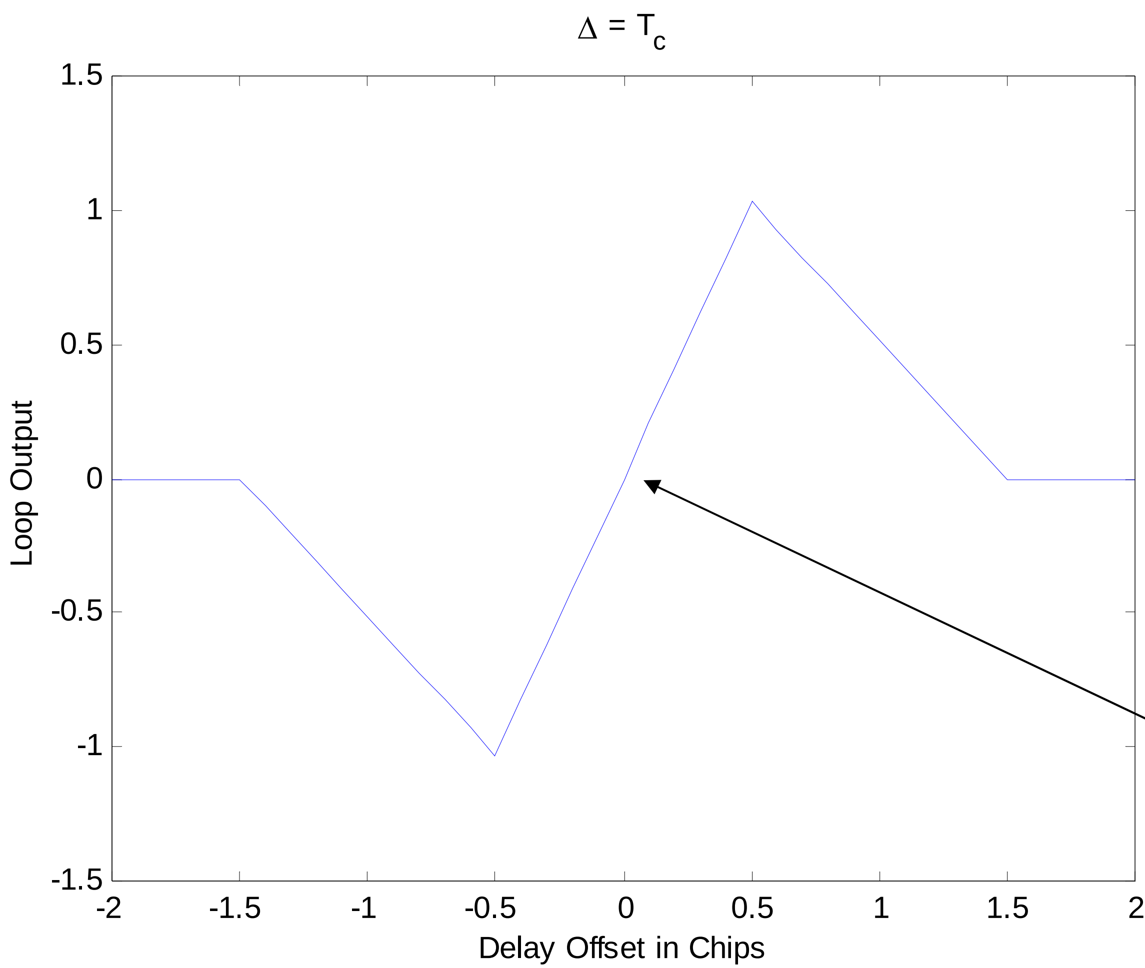


Coherent

$\Delta = \frac{1}{2} T_c$

Range = $-0.25T_c \leq \delta \leq 0.25T_c$

Delay Lock Loop : *S* - curve



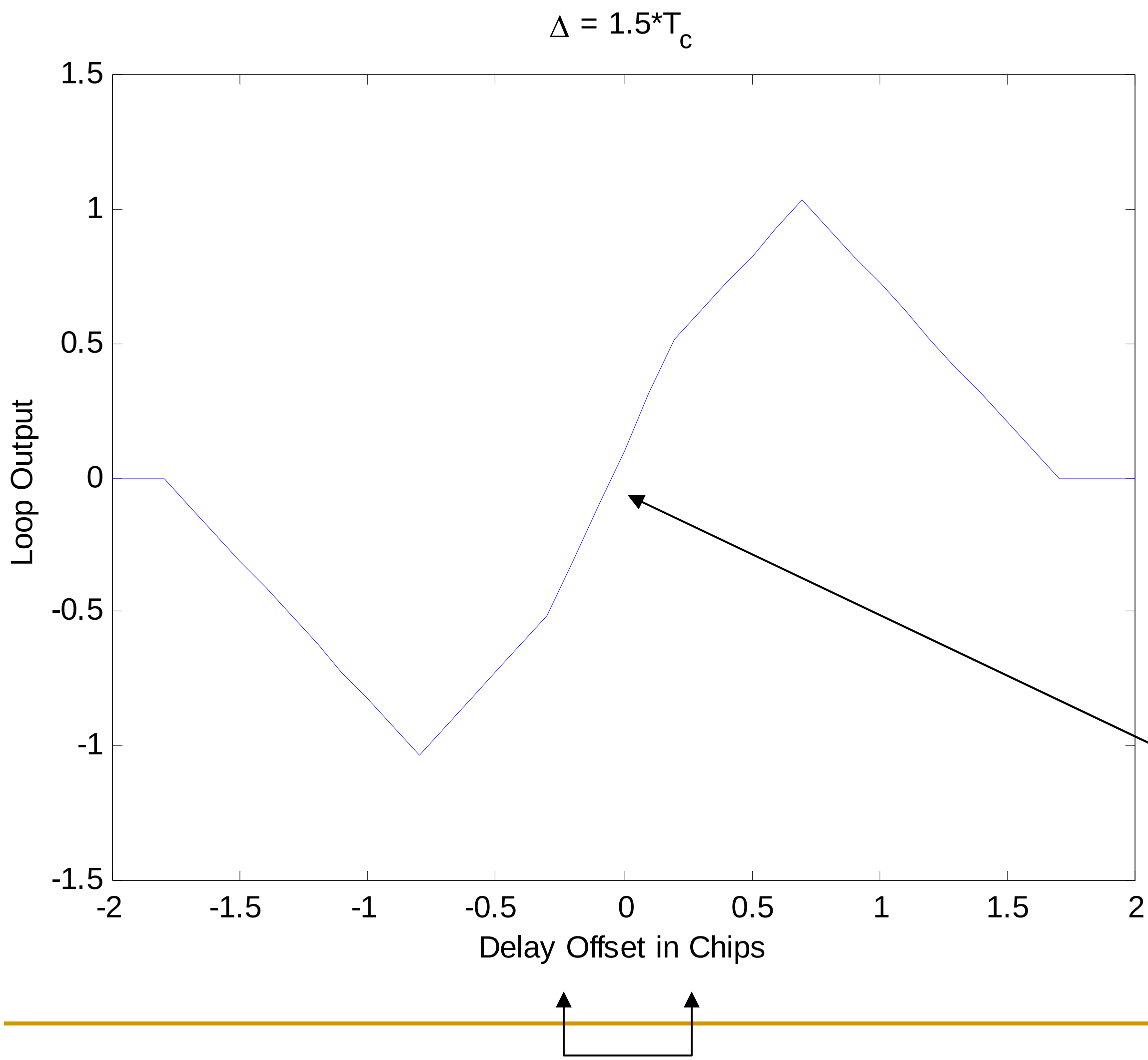
Coherent

$\Delta = T_c$

Slope = 2(1+1/N)

Range = $-0.5T_c \le \delta \le 0.5T_c$

Delay Lock Loop : S - curve



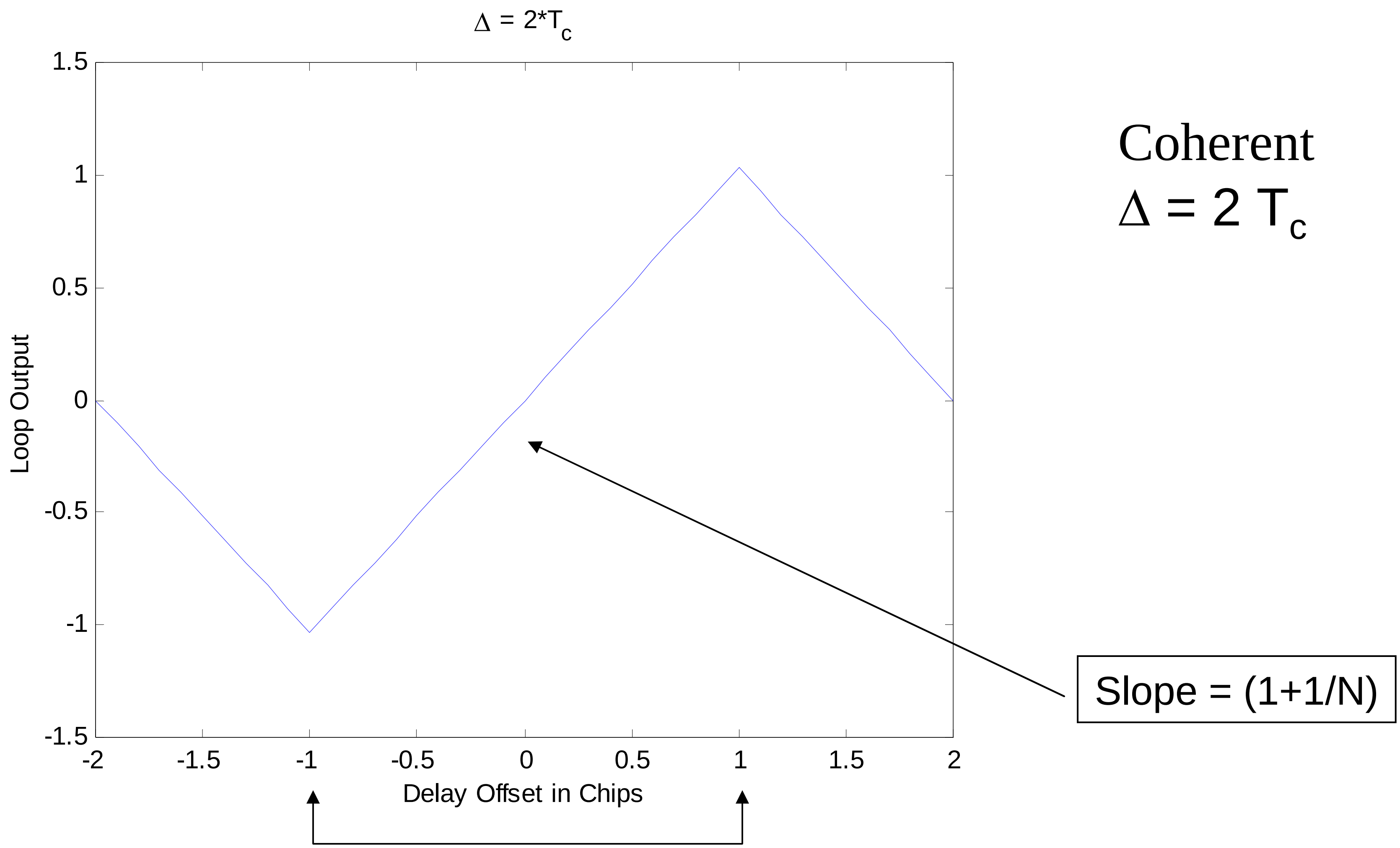
Coherent

$\Delta = 1.5\ T_c$

Slope = 2(1+1/N)

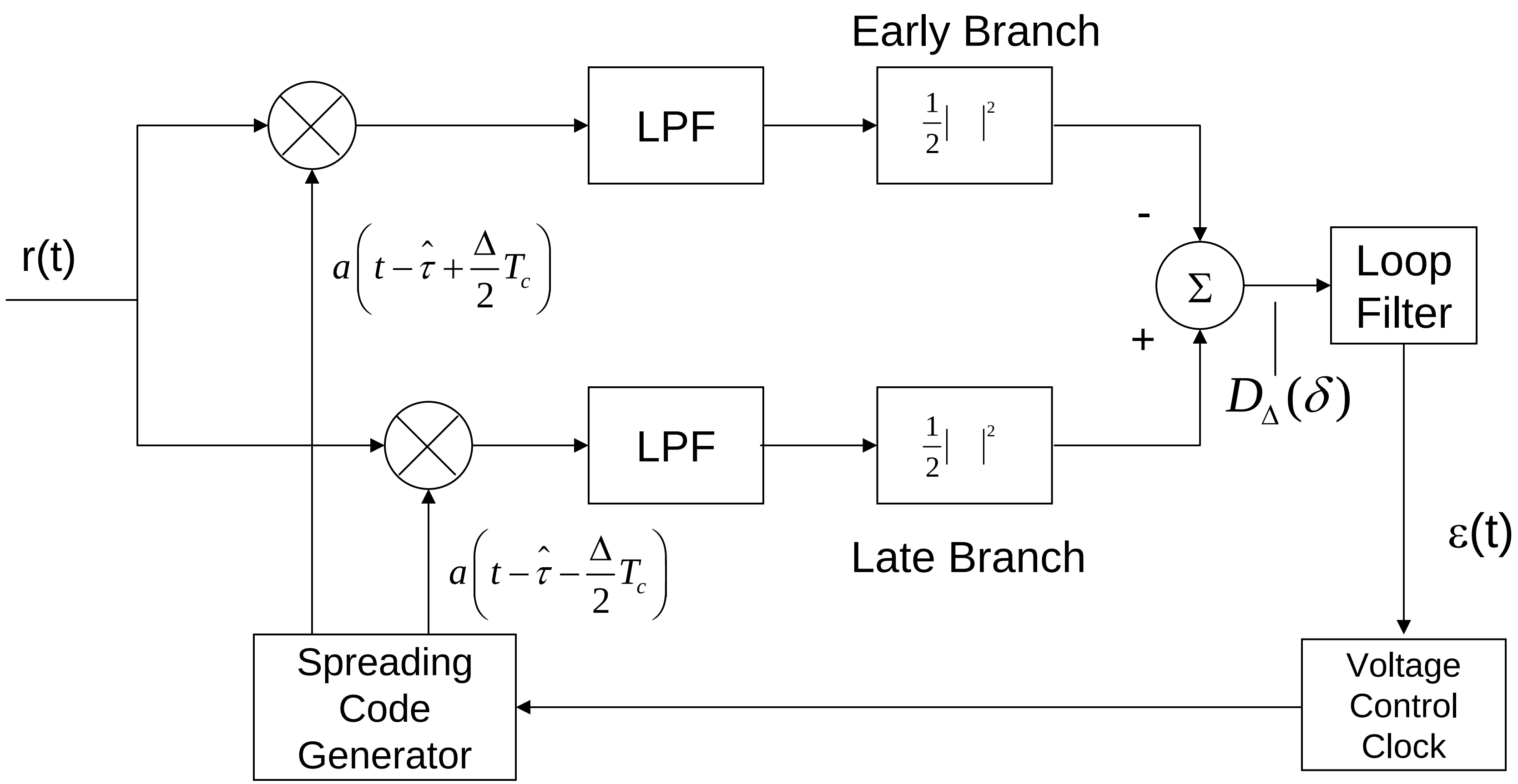
Range = $-0.25T_c \leq \delta \leq 0.25T_c$

Delay Lock Loop : *S* - curve



Range = $-T_c \leq \delta \leq T_c$

Non-Coherent Delay Lock Loop



- Non-coherent Early-Late Gate
  - Typically data modulation cannot be eliminated, thus we require a non-coherent loop.
  - This also allows for a residual phase/frequency offset.

Delay Lock Loop

- The output of the non-coherent Delay Lock Loop is

$$D_\Delta(\delta) = R_a^2\left[\left(\delta-\frac{\Delta}{2}\right)T_c\right] - R_a^2\left[\left(\delta+\frac{\Delta}{2}\right)T_c\right]$$

$$D_\Delta(\delta) = \begin{cases} 0 & -N+1+\frac{\Delta}{2} < \delta \le -\left(1+\frac{\Delta}{2}\right) \\ \frac{1}{N^2} - \left[1+\left(1+\frac{1}{N}\right)\left(\delta+\frac{\Delta}{2}\right)\right]^2 & -\left(1+\frac{\Delta}{2}\right) < \delta \le -\frac{\Delta}{2} \\ \frac{1}{N^2} - \left[1-\left(1+\frac{1}{N}\right)\left(\delta+\frac{\Delta}{2}\right)\right]^2 & -\frac{\Delta}{2} < \delta \le -\left(1-\frac{\Delta}{2}\right) \\ 2\left(1+\frac{1}{N}\right)\left[2-\left(1+\frac{1}{N}\right)\Delta\right]\delta & -\left(1-\frac{\Delta}{2}\right) < \delta \le \left(1-\frac{\Delta}{2}\right) \\ \left[1+\left(1+\frac{1}{N}\right)\left(\delta-\frac{\Delta}{2}\right)\right]^2 - \frac{1}{N^2} & \left(1-\frac{\Delta}{2}\right) < \delta \le \frac{\Delta}{2} \\ \left[1-\left(1+\frac{1}{N}\right)\left(\delta-\frac{\Delta}{2}\right)\right]^2 - \frac{1}{N^2} & \frac{\Delta}{2} < \delta \le \left(1+\frac{\Delta}{2}\right) \end{cases}$$

$\Delta >= 1$

For small δ, and $\Delta=1$

$$D_\Delta(\delta) = 2\left(1+\frac{1}{N}\right)\left[2-\left(1+\frac{1}{N}\right)\right]\delta$$
$$\approx 2\delta$$

Delay Lock Loop

- The output of the non-coherent Delay Lock Loop is

$$D_\Delta(\delta) = R_a^2\left[\left(\delta - \frac{\Delta}{2}\right)T_c\right] - R_a^2\left[\left(\delta + \frac{\Delta}{2}\right)T_c\right]$$

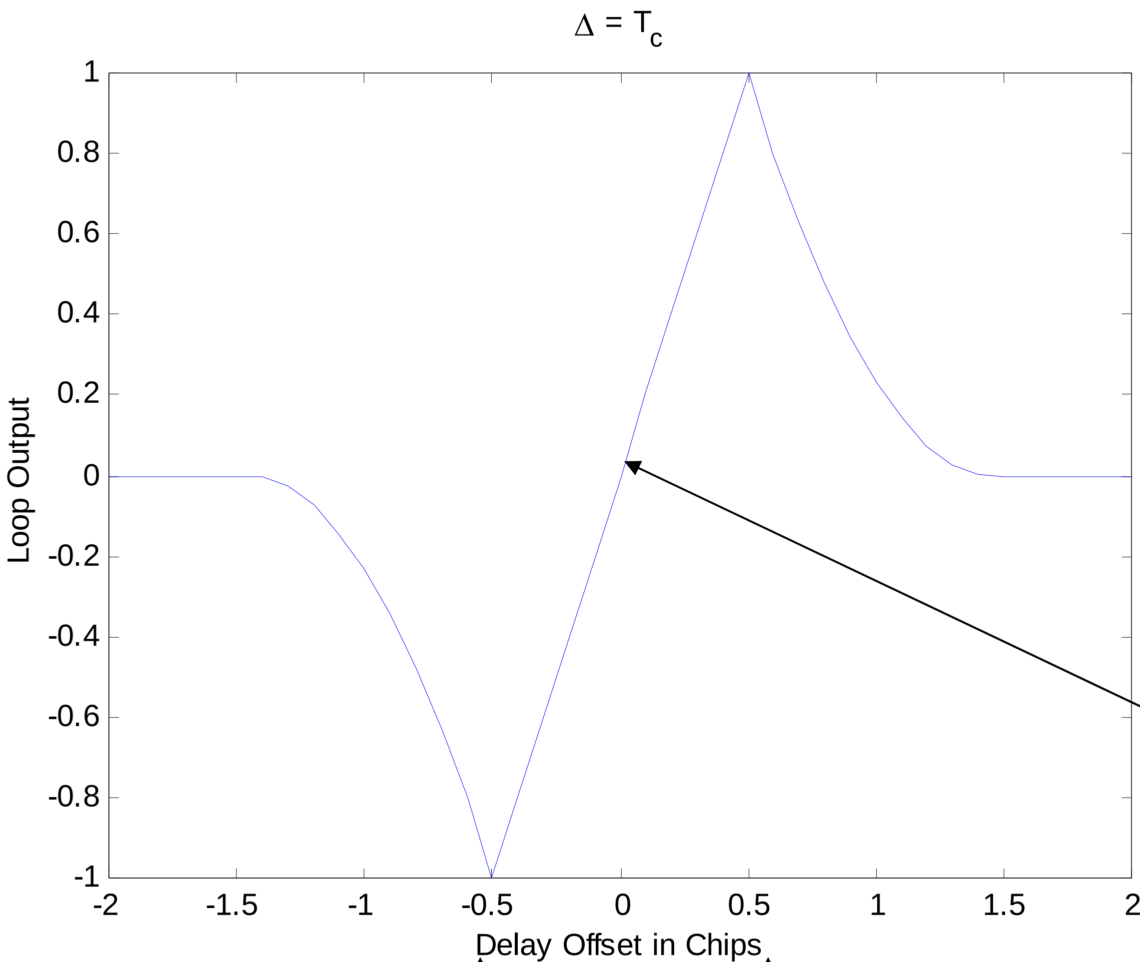
$$D_\Delta(\delta) = \begin{cases} 0 & -N+1+\frac{\Delta}{2} < \delta \le -\left(1+\frac{\Delta}{2}\right) \\ \frac{1}{N^2} - \left[1+\left(1+\frac{1}{N}\right)\left(\delta+\frac{\Delta}{2}\right)\right]^2 & -\left(1+\frac{\Delta}{2}\right) < \delta \le -\left(1-\frac{\Delta}{2}\right) \\ -2\left(1+\frac{1}{N}\right)\Delta\left[1+\left(1+\frac{1}{N}\right)\delta\right] & -\left(1-\frac{\Delta}{2}\right) < \delta \le -\frac{\Delta}{2} \\ 2\left(1+\frac{1}{N}\right)\left[2-\left(1+\frac{1}{N}\right)\Delta\right]\delta & -\frac{\Delta}{2} < \delta \le \frac{\Delta}{2} \\ 2\left(1+\frac{1}{N}\right)\Delta\left[1-\left(1+\frac{1}{N}\right)\delta\right] & \frac{\Delta}{2} < \delta \le \left(1-\frac{\Delta}{2}\right) \\ \left[1-\left(1+\frac{1}{N}\right)\left(\delta-\frac{\Delta}{2}\right)\right]^2 - \frac{1}{N^2} & \left(1-\frac{\Delta}{2}\right) < \delta \le \left(1+\frac{\Delta}{2}\right) \end{cases}$$

Δ<=1

For small δ, and Δ=1

$$D_\Delta(\delta) = 2\left(1+\frac{1}{N}\right)\left[2-\left(1+\frac{1}{N}\right)\right]\delta \approx 2\delta$$

Delay Lock Loop



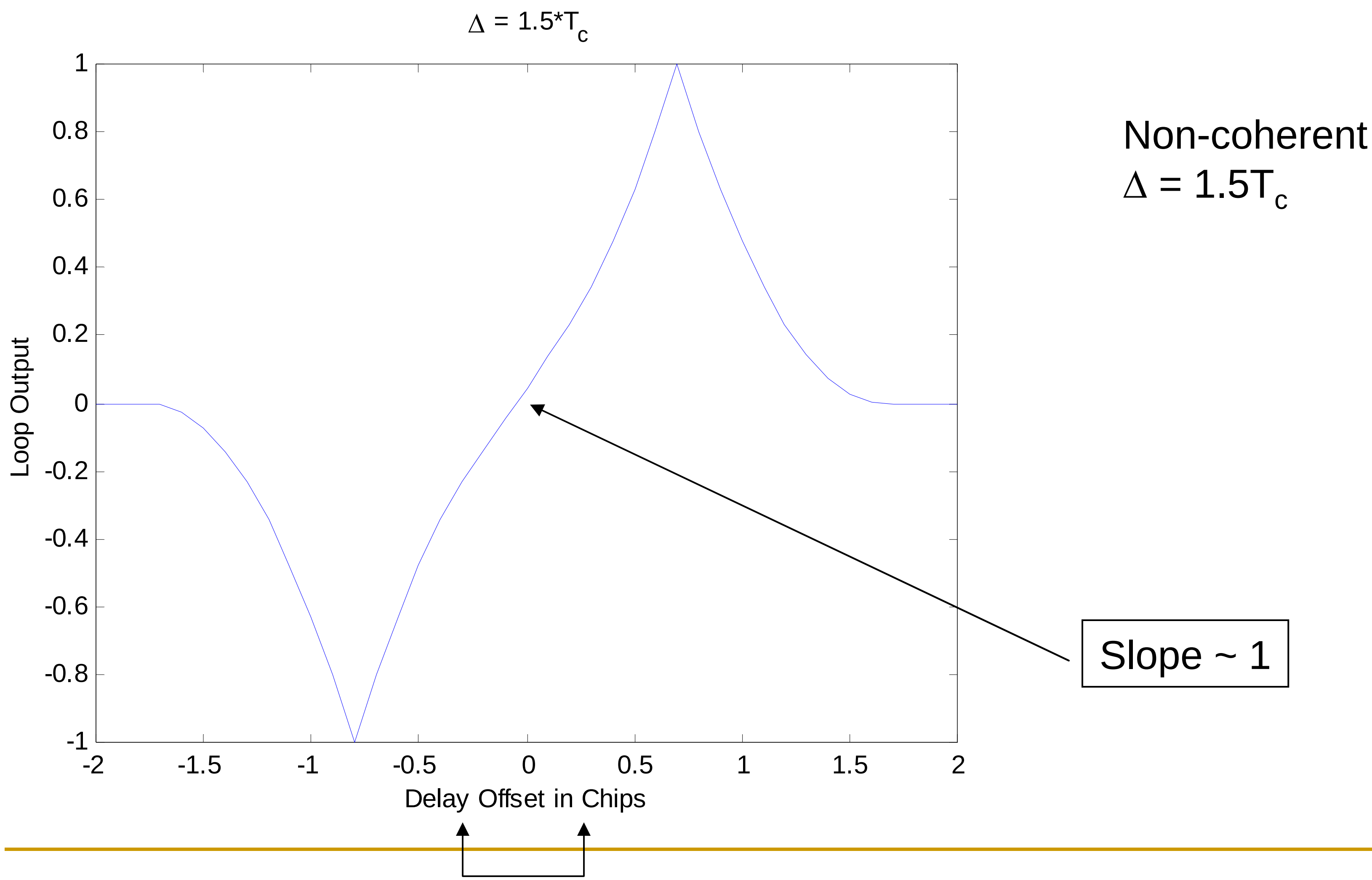
Non-coherent

$\Delta = T_c$

Slope = $2(1+1/N)^2$

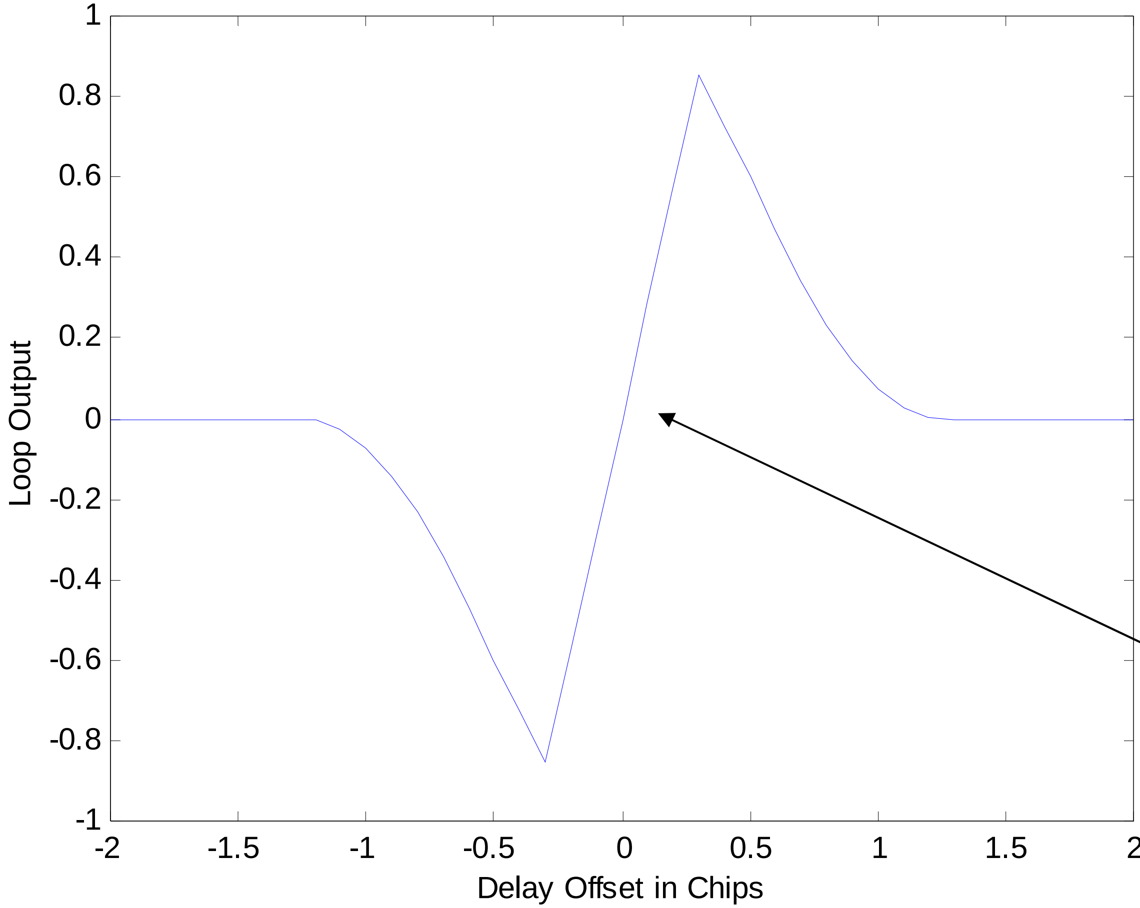
Range = $-0.5T_c \leq \delta \leq 0.5T_c$

Delay Lock Loop



Range = $-0.25T_c \le \delta \le 0.25T_c$

Delay Lock Loop

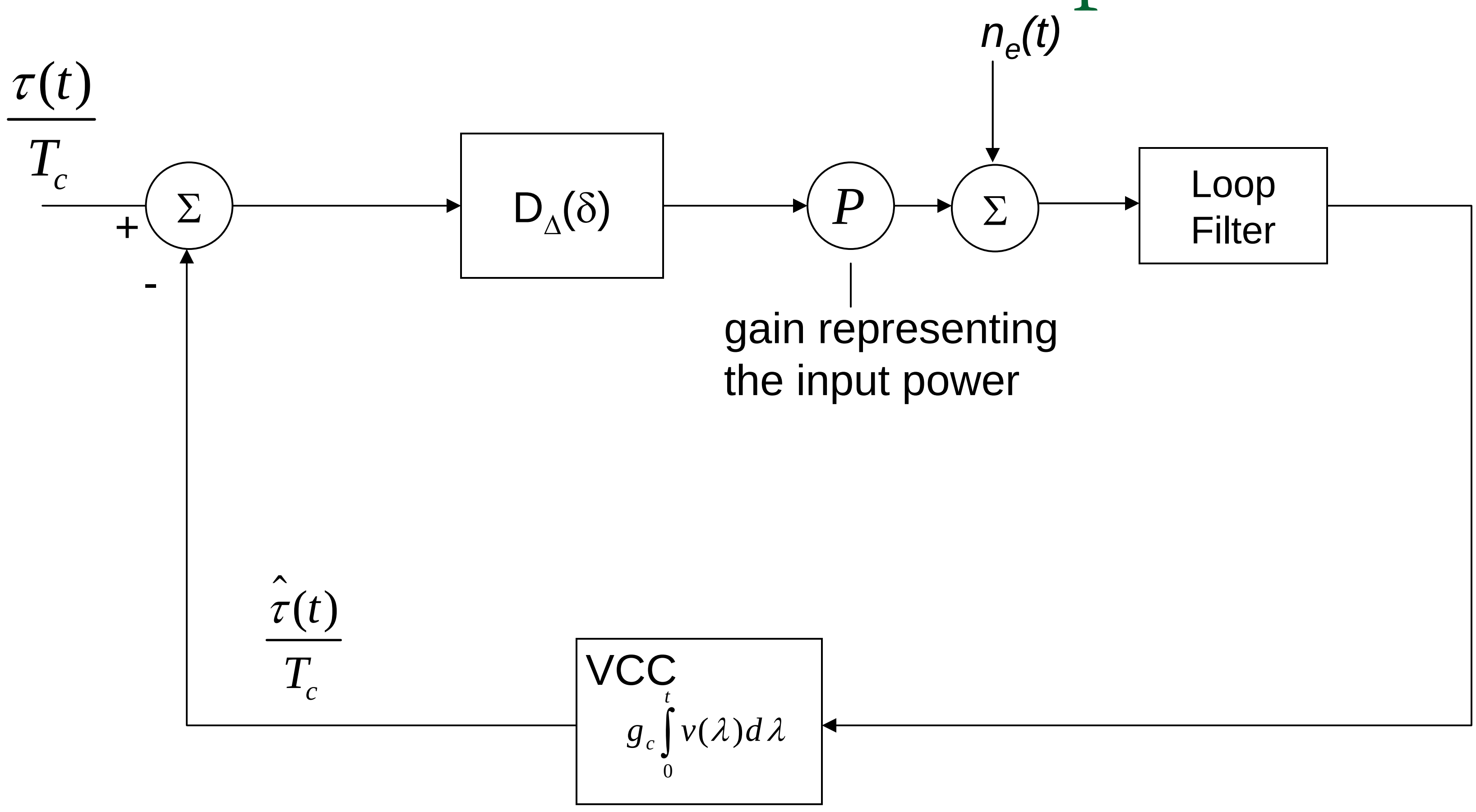


Non-coherent
$\Delta = 2/3T_c$

Slope ~ 8/3

Range $= -0.125T_c \leq \delta \leq 0.125T_c$

Non-linear Model of Loop



$n_e(t)$ is low pass Gaussian noise
$\tau(t)$ is the time varying delay of the input signal
T_c is the chip duration

Linear Model

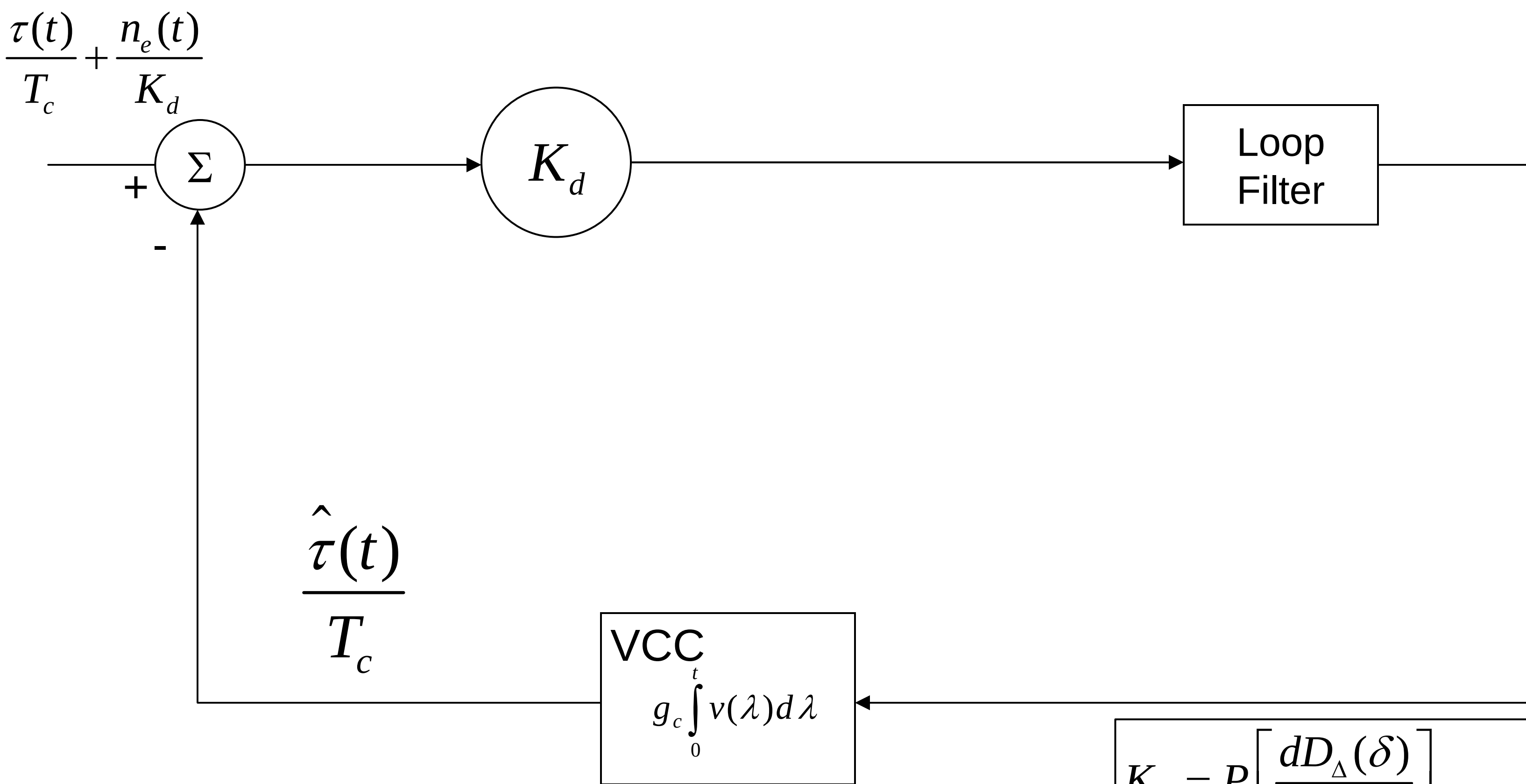
- For small error, δ, the discriminator *S*-curve can be approximated as linear

$$D_{\Delta}(\delta) = 4\left(1+\frac{1}{N}\right)\left[1-\left(1+\frac{1}{N}\right)\frac{\Delta}{2}\right]\delta$$

- We can lump together the gains from the signal power and the discriminator to form a single gain K_d and move the noise to the input (since it is now a linear loop)

$$K_d = 4P\left(1+\frac{1}{N}\right)\left[1-\left(1+\frac{1}{N}\right)\frac{\Delta}{2}\right]$$

Linear Model



$$K_d = P\left[\frac{dD_\Delta(\delta)}{d\delta}\right]_{\delta=0} = 4P\left(1+\frac{1}{N}\right)\left[1-\left(1+\frac{1}{N}\right)\frac{\Delta}{2}\right]$$

$n_e(t)$ is low pass Gaussian noise
$\tau(t)$ is the time varying delay of the input signal
T_c is the chip duration

Loop Analysis

- Let the loop filter be $\alpha F(z)$, and the accumulator is modeled as $\frac{z^{-1}}{1-z^{-1}}$ then

$$\frac{\hat{\tau}(z)}{T_c} = \left(\frac{\tau(z)}{T_c} - \frac{\hat{\tau}(z)}{T_c}\right)\frac{\alpha K_d F(z) z^{-1}}{1-z^{-1}}$$

$$\frac{\hat{\tau}(z)}{T_c} = \frac{\tau(z)}{T_c}\frac{\frac{\alpha K_d F(z) z^{-1}}{1-z^{-1}}}{1+\frac{\alpha K_d F(z) z^{-1}}{1-z^{-1}}}$$

$$= \frac{\tau(z)}{T_c}\frac{H(z)}{1+H(z)}$$

- Now, if we let *F(z)* = 1,

$$\frac{\hat{\tau}(z)}{T_c} = \frac{\tau(z)}{T_c}\frac{\frac{\alpha K_d z^{-1}}{1-z^{-1}}}{1+\frac{\alpha K_d z^{-1}}{1-z^{-1}}}$$

$$= \frac{\tau(z)}{T_c}\frac{\alpha K_d z^{-1}}{1-z^{-1}\left(1-\alpha K_d\right)}$$

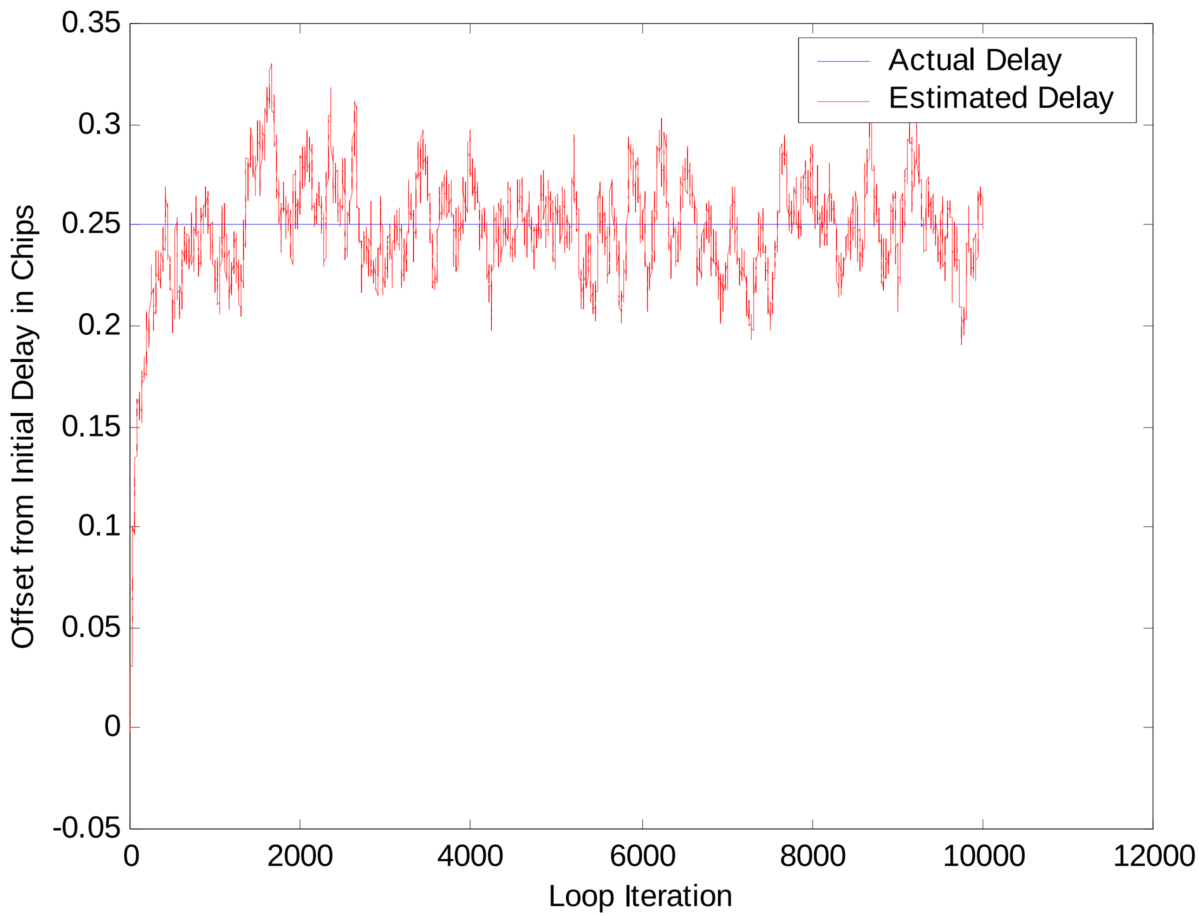
Loop Analysis (cont.)

- Now, for $\Delta = T_c$
$$K_d = 4P\left(1+\frac{1}{N}\right)\left[1-\left(1+\frac{1}{N}\right)\frac{\Delta}{2}\right]$$
$$\approx 2P$$
$$\frac{\hat{\tau}(z)}{T_c} = \frac{\tau(z)}{T_c}\frac{\alpha 2Pz^{-1}}{1-z^{-1}\left(1-2\alpha P\right)}$$

- *And the error response is*
$$\tau_e(z) = \left(\frac{\tau(z)}{T_c} - \frac{\hat{\tau}(z)}{T_c}\right) = \frac{\tau(z)}{T_c}\frac{1-z^{-1}}{1-z^{-1}\left(1-2\alpha P\right)}$$

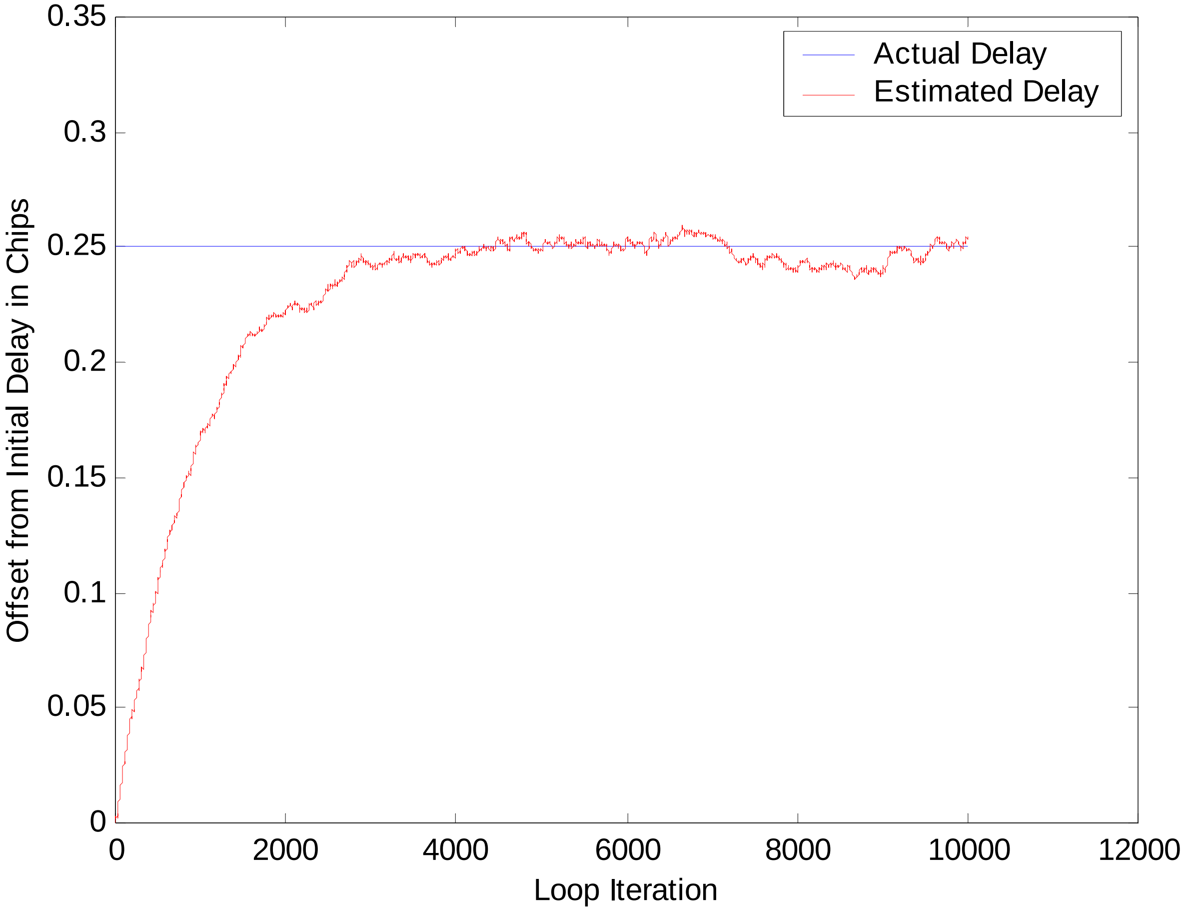
- *P* represents the input signal power and α is the update constant. The smaller the value of α, the slower the tracking ability of the DLL, but the lower the jitter due to noise. For a step change of $\Delta\tau/T_c$ we obtain
$$\tau_e(z) = \frac{\Delta\tau}{T_c}\frac{1}{1-z^{-1}}\frac{1-z^{-1}}{1-z^{-1}\left(1-2\alpha P\right)} = \frac{\Delta\tau}{T_c}\frac{1}{1-z^{-1}\left(1-2\alpha P\right)}$$

Example



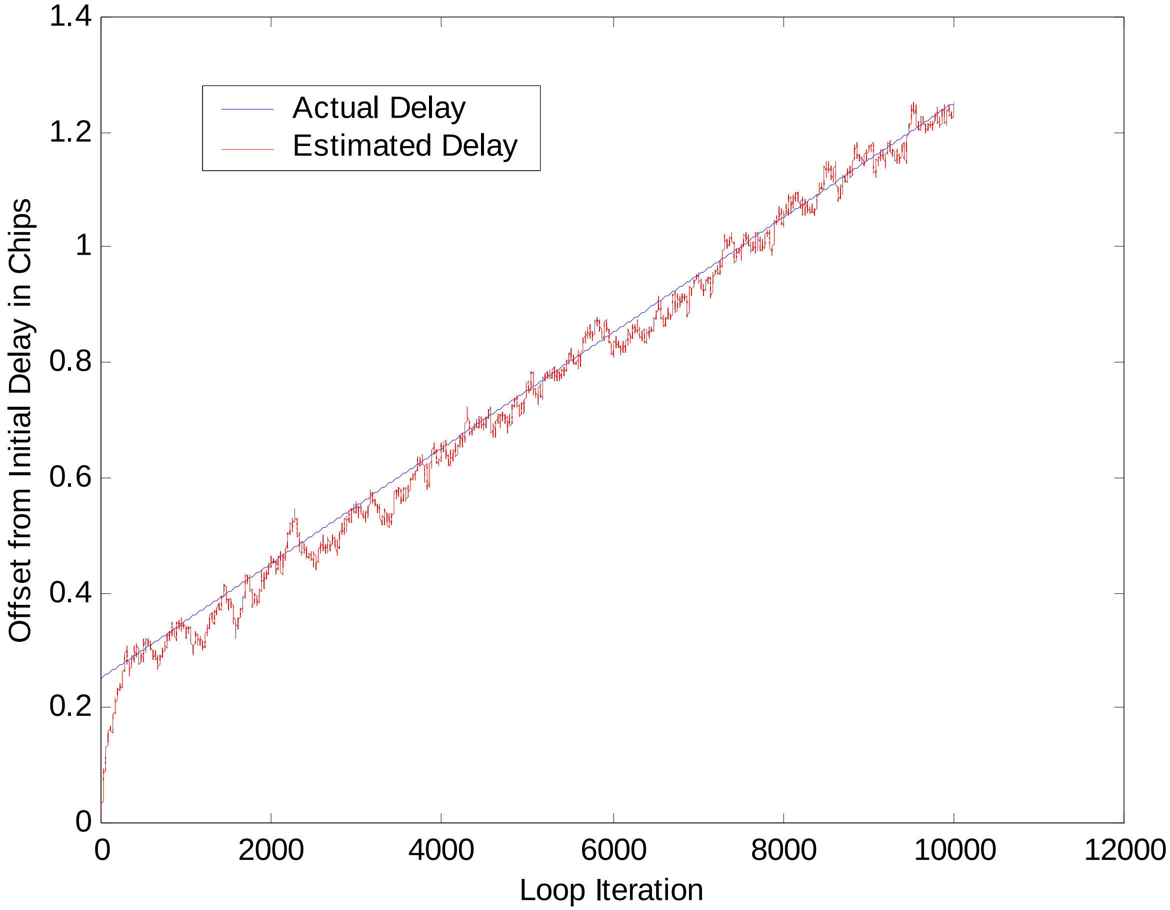
- α = 0.01
- SNR = 10dB
- Constant delay

Example



- $\alpha = 0.001$
- SNR = 10dB
- Constant delay

Example



- α = 0.01
- SNR = 10dB
- Slew rate = 0.0001 samples/sample

Other Tracking Loops

- Tau-Dither Non-coherent Tracking Loop
- Double Dither Non-coherent Tracking Loop

Conclusions

- Today we have discussed the second aspect of code synchronization which is termed *tracking*
  - Fine-tunes delay estimate
- Most common approach to tracking is the Delay-Lock Loop
- The performance of the DLL depends on the loop bandwidth and characteristics of the loop *S*-curve